Multi-DSP Parallel Processing Platform for Hyperspectral Anomaly Detection*

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Abstract. To satisfy the aerospace requirements of high speed and huge data processing etc., this paper proposes a solution of multi-DSP parallel processing platform based on CPCI Express standard bus architecture for hyperspectral anomaly detection onboard. The hardware topological architecture of the platform combines the tight coupling of four DSPs sharing data bus and memory unit with the interconnection of Link ports. On this hardware platform, by assigning parallel processing mission for each DSP in consideration of the anomaly detection algorithm and the spectral features, a parallel processing method which conducts matrix computations of the whole image by spatially partitioning the image is proposed. The experimental results show that, in the case of equivalent detection effects, the proposed 4-DSP parallel processing system can reach the time efficiency of 4 times than the single DSP system for hyperspectral anomaly detection, which makes a breakthrough in the constraints to the huge data processing of DSPs internal storage capacity, meanwhile well meeting the demands of onboard hyperspectral data processing.

Keywords: Parallel processing, Multi-DSP, Hyperspectral data, Anomaly detection

1 Introduction

With relatively high spectral resolution, the hyperspectral data provide a powerful basis for distinguishing diverse substances which exist subtle spectral differences. With respect to conventional image, the hyperspectral data are superior in target detection and recognition, widely applied to many areas including environmental monitoring, urban planning, disaster evaluation, and agricultural production, and has become a leading research direction in automotive target recognition field[1]. The spectral anomaly detection algorithm[2][3] can detect the target whose spectrum is different from its surrounding background without prior spectral information, thus has very strong practicability.

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By collecting spatial and spectral information at the same time, the hyperspectral data are remarkably complex and massive, which lead to the urgent demands for high-performance computing[4], especially when it is applied to the onboard data processing in aerospace remote sensing, which needs high-speed data transmission, real-time processing and large storage capacities etc.

In recent years, many research institutions have conducted a lot of studies on real-time processing technology for spectroscopic data, by adopting a variety of hardware platforms such as CPUGPU multi-core processor[5], FPGA+ multi-DSP parallel architecture[6], respectively. For the spaceborne or airborne hyperspectral data processing, it has become the main trend to use multi-DSP parallel architecture as the onboard data processing system[6-8]. Such DSP-based embedded system can resist the complex and severe space environment and the parallel processing system can achieve better real-time capability and high precision, which has not only broken the improvement limit of single-processor performance, but also effectively improved the compatibility and the upgrade ability of the system.

Under background of aerospace application of onboard hyperspectral data processing[9], this paper presents a solution of embedded hyperspectral data processing platform based on multi-DSP and FPGAs architecture with CPCI Express standard bus. The hardware structure combines the tight coupling of four DSPs (TS201) sharing bus and the memory with the interconnection of LVDS (low voltage differential signal) LINK ports, which has excellent parallel processing capability and high-efficient data transmission ability, and is suitable for onboard hyperspectral data processing, which needs high parallelism and heavy computation. In order to conduct the anomaly detection on the hardware platform mentioned above, this paper proposes a parallel anomaly detection algorithm by dividing the time-consuming computation of the whole image into data blocks computation. Compared with ground processing platform based on one single core CPU, the 4-Dsps processing platform proposed in this paper ran a little faster than the processing speed of 2.83 GHz CPU platform.

2 Parallel Hardware Platform

The processing system capacity is depending on the DSP performance. The complicated spectral data processing algorithm requires large amounts of floating point arithmetic, as we know, ADI Tiger-SHARC processor ADSP-TS201S is designed for floating point computation, which also has 24Mbit SRAM and 600MHz CCLK(core clock), and reaches 3.6 GFLOPs processing ability. Therefore the ADSP-TS201S Dsp is selected as the processor. Moreover, each DSP has 4 channels of Link ports and each channel has a data transmission rate up to 4Gbps, providing high-speed seamless connection to multi-DSP parallel processing.

The performance of the multi-DSP parallel processing platform is depending on the platform topological architecture, parallel processing algorithm and mission assignment method. These three items are closely connected to and de-

pending on each other. The platform topological architecture generally includes two types: one is the shared-bus or shared-storage system, named tight coupling parallel system; the other one is the distributed parallel system or loose coupling system, in which each processing unit has respectively independent storage unit and is connected by communication ports.

The parallel hardware platform presented in this paper is based on CPCI Express standard bus architecture, and Four ADSP-TS201S Dsps are composed into a DSP cluster, as a core parallel processing unit, which also includes FPGA, SDRAM, FLASH and PCI bus-bridge. The four DSPs combine the topological architecture of shared-bus tight coupling with the interconnection of Link ports, which realize the synchronization and mutual communication of DSPs, while the external CPCI bus realizes spectral data transmission. Figure 1 shows the framework of the bus connection. As shown in Fig. 1, each DSP has a unique identification (ID) and maps its address to the sharing memory SDRAM. The DSP cluster forms a loop circuit by Link ports inside, and the other Link ports are connected to FPGA. Figure 2 shows the framework of the Link ports interconnection inside the cluster.

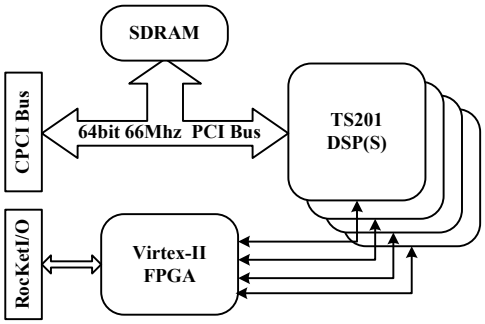

Fig. 1. Framework of the system bus connection.

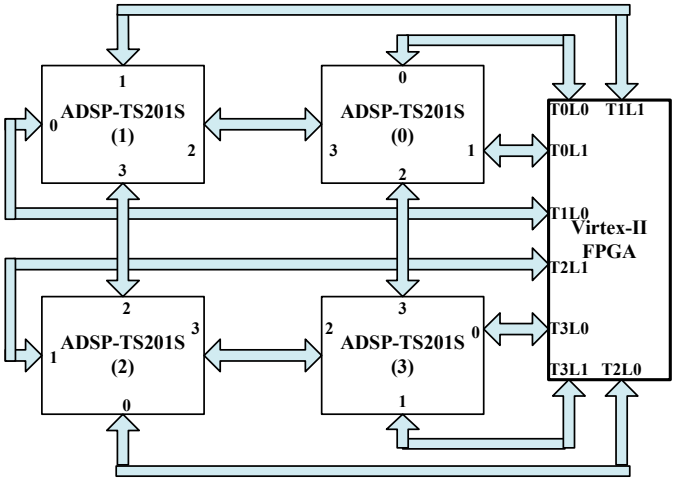

Fig. 2. Framework of the Link port connections inside a DSP cluster.

3 Parallel Realization of Anomaly Detection

RX detector is known as a classic algorithm in hyperspectral anomaly detection[10], and is a constant false alarm rate detection algorithm based on Generalized Likelihood Ratio Test, which only needs to estimate background covariance matrix without knowing the target spectral information, and has already been applied in many hyperspectral anomaly detections successfully. Figure 3 shows the flow chart of RX anomaly detection algorithm based on a single DSP.

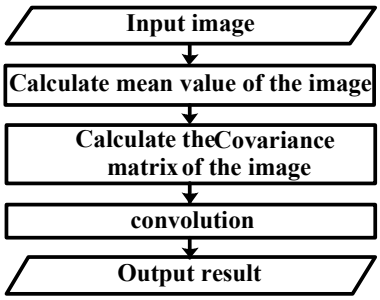

Fig. 3. RX anomaly detection algorithm based on a single DSP.

Based on the multi-DSP hardware platform described above, how to realize the parallel mission assignment among DSPs becomes the main task for the parallel processing of RX anomaly detection, which mostly affects time-cost of the whole system. There are usually two kinds of parallel processing strategies: one is to divide the whole algorithm into several parts, and each DSP calculates one part of the algorithm, similar to DSP software pipelining; another is to partition the source data, and each DSP computes one data block in parallel. The first parallel strategy is suitable for the algorithm easy to be divided into multiple program segments with equal processing time, and often applied to communication signals processing. Upon analyzing the whole RX detection procedure, its obvious to find that the covariance matrix computation of the input data is the most time-consuming part and is difficult to be divided, while the computations of the mean value matrix and covariance matrix of the input data are both related to the gray values of spatial pixels in each data block, therefore the second parallel processing strategy is fit for the RX detection algorithm, i.e., partitioning the source data into blocks, and computing those data blocks by respective DSPs in parallel form. Figure 4 shows the flow chart of the parallel processing of the RX algorithm. Compared to the single-DSP process in figure 3, the source data are firstly partitioned by spatial dimension, and then four DSPs co-process the data blocks. Theoretically, the 4-DSP parallel processing can reach the time efficiency of 4 times than the single-DSP processing. But normally, because of the coordination and processing delay among multi-DSP and bus competition, the actual processing speed is less than 4 times.

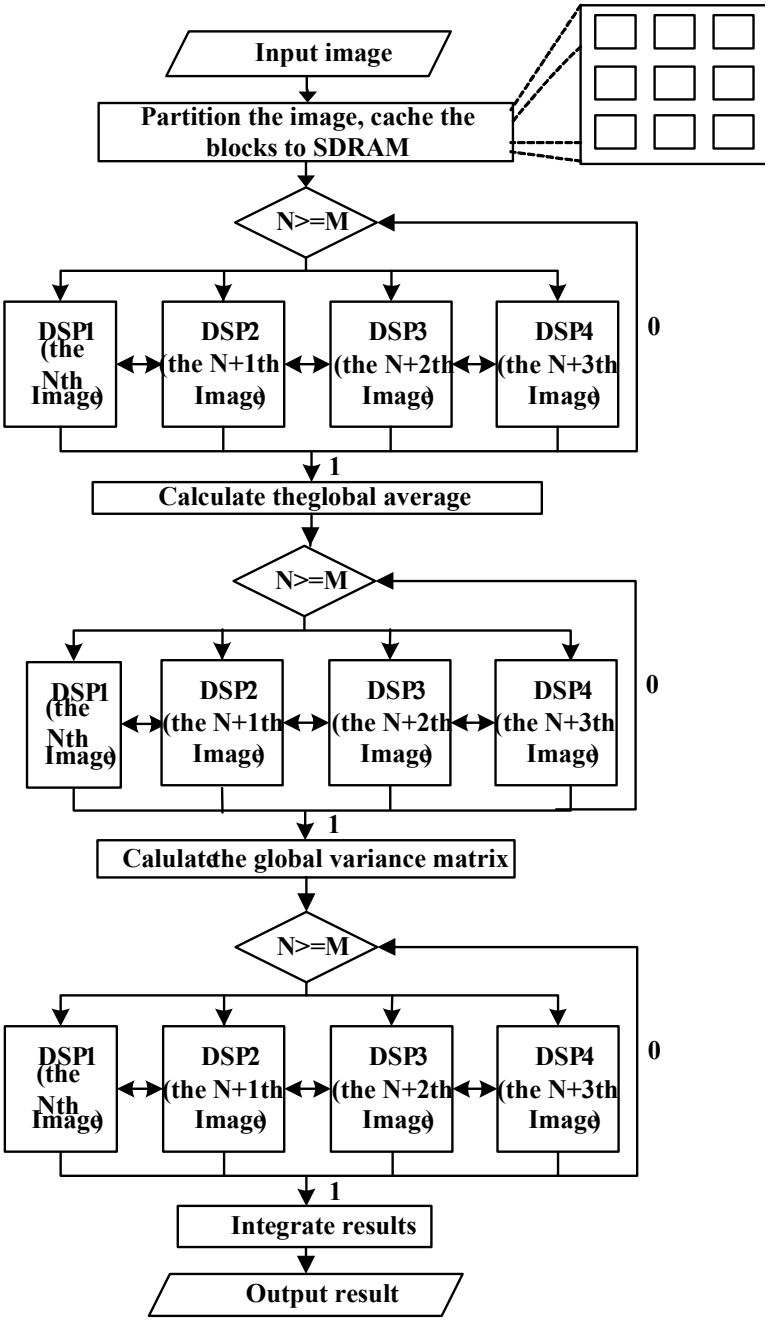

Fig. 4. RX anomaly detection parallel procedure based on 4-DSP.

During the procedure in Fig.4, firstly, the spectral data cube is partitioned by spatial dimension into M blocks, and put them into SDRAM. Secondly, a global variable N (N starts from 1) is defined as the number of readout data blocks. Each DSP reads a block into the internal storage successively, meanwhile notifies the other three DSPs of a variable value N+1 through the circular LINK ports, and then processes the block in the internal storage. When any piece of DSP completes the processing, it reads another block to be processed from SDRAM according to the N value, until the entire data processing is completed. The computation results are cumulated. Finally, the mean value matrix and covariance matrix of the source data are obtained by the accumulation of each DSPs computation results.

For the structure of accessing the storage by shared bus, it will cause bus competition problem when DSP reads data and stores results. Therefore an appropriate bus arbitration mechanism can solve the bus competition problem and improve the efficiency of multi-DSP parallelization. The bus arbitration mechanism of fixed priority and introducing delay are adopted to the parallel processing, i.e., among the four DSPs, DSP0 is on the top of the fixed priority list, and the next is DSP1, the last is DSP3. In the parallel procedure, each DSP should inquire the bus status (free or busy) first to access the data bus. DSP0 notifies DSP1, DSP2 and DSP3, successively, of the bus status busy and the number of data block to be read through the Link ports, and then reads the first block, after which informs each DSP of the bus status free successively. As shown in Figure 5, since DSP1 first receives the status free from DSP0, DSP1 will immediately inform the other three DSPs that the bus is busy and the number of image block (the second block) to be read, ensuring that DSP2 and DSP3 receive the bus status busy from DSP1 before they receive the status free from DSP0 by introducing delay, so that the bus competition problem is solved.

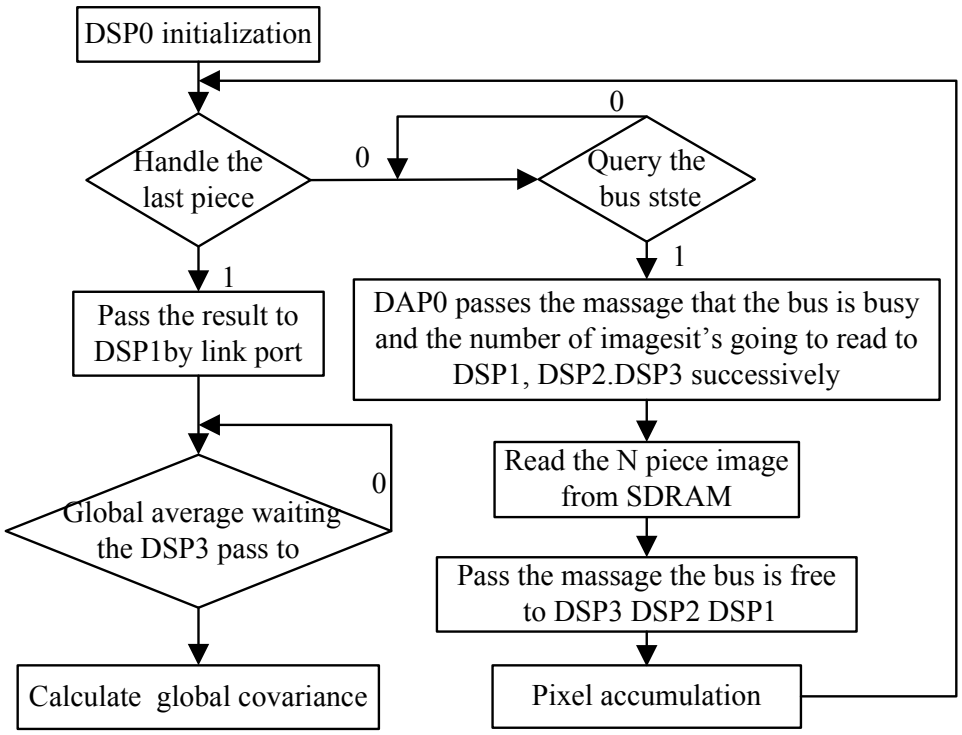

Fig. 5. The flow chart of the bus arbitration mechanism used in this paper.

4 Experimental results and analysis

The experimental hyperspectral data were acquired by the HyMap airborne hyperspectral sensor from Cooke City of Montana in July 2006[11]. The ground resolution of HyMap sensor is 3 meters, the spectral range is 450nm -2500nm with 126 spectral bands, the size of data cube is 800 (pixels) *280 (pixels) *126 (bands). Figure 6 shows the original hyperspectral image. Based on the RX anomaly detection parallel algorithm and 4-DSP processing platform introduced above, the paper conducted three comparative experiments: single-DSP anomaly detection, 4-DSP parallel detection and single-core CPU detection. Figure 7 shows the RX anomaly detection results under the three kinds of hardware platforms.

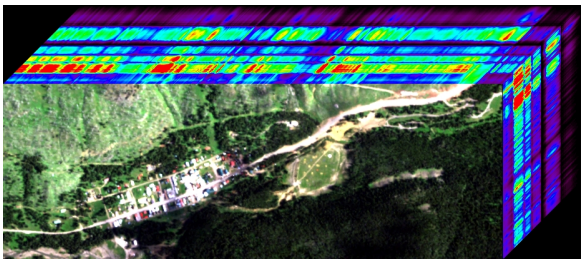

Fig. 6. Original hyperspectral data (800 * 280 * 126).

The experimental result indicates that: the detection effects of RX anomaly detection algorithm achieved by the three platform of single-DSP, 4-DSP and single-core CPU are very similar, wherein the number of anomaly targets detected by CPU are a bit more than that by single-DSP and 4-DSP. Table 1 shows the comparison of the processing time-cost for the single-DSP, 4-DSP and single-core CPU. It can be found that, 4-DSPs parallel platform (the processing time is 50.342s) not only achieve the time efficiency of 4 times than single-DSP processing, which requires 198.643s, but also get a processing speed comparable with the single-core CPU with main frequency 2.83GHz. The experimental results above indicate that the proposed multi-DSP parallel platform reaches the aim for hyperspectral anomaly detection, and well satisfies demands for onboard spectral data processing.

Table 1. Comparisons of processing time among single-DSP, 4-DSP and single-core CPU

$ProcessorType$	$SingleDSP$	$4-DSP$	$SinglecoreCPU$
Processing Time(s)	198.643	50.342	55

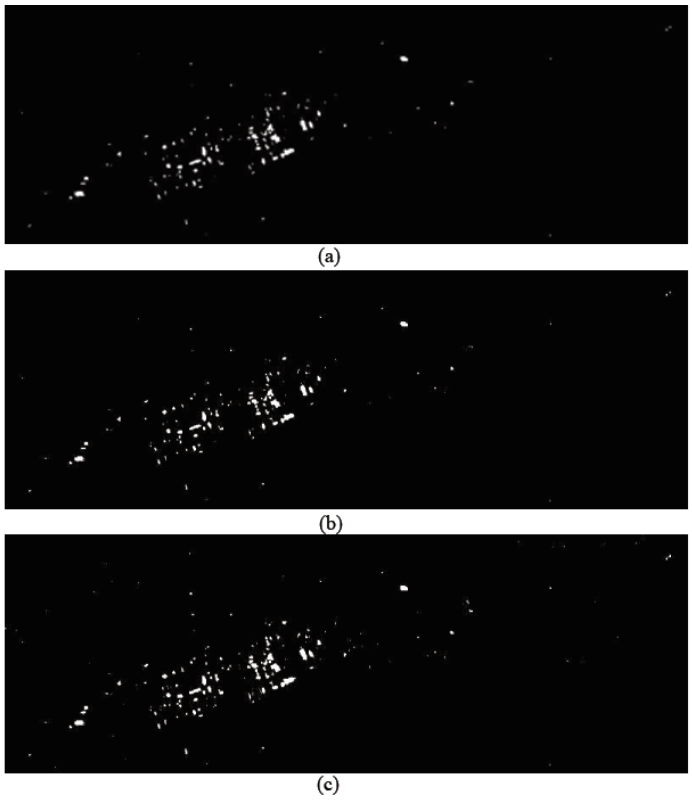

Fig. 7. (a) RX anomaly detection result based on single-DSP (b) RX anomaly detection result based on 4-DSP (c) RX anomaly detection result based on single-core CPU

5 Conclusion

This paper proposes a multi-DSP parallel processing platform for hyperspectral anomaly detection based on the CPCI Express standard bus architecture. The platform excellently solves the issues of real-time and huge data for the hyperspectral data processing by means of parallel strategy for RX algorithm, the parallel mission assignment and the sharing bus arbitration mechanism. This paper mainly discusses the parallel realization of anomaly detection and realizes the parallel processing of RX anomaly detection. In the future many follow-up works such as the detection rate and false alarm rate of the detection results, the automatic threshold segmentation of anomaly points, and the extraction of the target characteristic spectrum still need further in-depth study.

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