1. Motivation

- Multicore processors use a shared system bus to fetch data/instructions from main memory.
- This sharing can cause non-deterministic variations in the tasks’ execution times due to inter-task bus blocking.
- Phased execution models, e.g., 3-phase task model, are promising candidates to circumvent the problem of inter-task bus blocking.
- State-of-the-art bus contention analyses for 3-phase tasks only focus on global scheduling.

2. Contributions

- Bus blocking-aware WCRT analysis for the 3-phase task model under partitioned non-preemptive scheduling.

3. Level-i Busy Window

- Level-i busy window \( W_{li} \) of core \( \pi_i \) is given by:
  \[
  W_{li} = C_{pi}^{\text{Max,li}} + B_{pi}^{\text{Max,li}}(W_{li}) + \sum_{j \in \text{hep}_{pi}} \left( \eta_j(\pi_i)(W_{li}) \right) C_{pi}
  \]
- Max. blocking from \( I_{pii} \)
- Max. interference from \( \text{hep}_{pi} \)
- Max. number of jobs of task \( \tau_i \) that can execute in \( W_{li} \):
  \[
  \eta_i(\pi_i)(W_{li})
  \]

4. Computing Bus Blocking

- The maximum bus blocking \( B_{\text{bus}}(W_{li}) \) suffered by the tasks of local core \( \pi_i \) from the tasks of remote core \( \pi_r \) in any time window of length \( W_{li} \) depends on:
  - The maximum number of times the jobs released on the local core \( \pi_i \) can suffer bus blocking in \( W_{li} \), i.e., \( N_{\pi_i}(W_{li}) \).
  - The maximum number of times the jobs released on the remote core \( \pi_r \) can suffer bus blocking in \( W_{li} \), i.e., \( N_{\pi_r}(W_{li}) \).
- There are three possible cases:

   **Case 1:** \( N_{\pi_i}(W_{li}) > N_{\pi_r}(W_{li}) \)
   - \( B_{\text{bus}}(W_{li}) \) is given by the sum of the execution time of all memory phases of all jobs released on core \( \pi_r \) in \( W_{li} \).

   **Case 2:** \( N_{\pi_i}(W_{li}) = N_{\pi_r}(W_{li}) \)
   - \( B_{\text{bus}}(W_{li}) \) is given by the sum of all memory phases of all jobs (except the smallest A- or R-phase) of core \( \pi_r \) in \( W_{li} \).

   **Case 3:** \( N_{\pi_i}(W_{li}) < N_{\pi_r}(W_{li}) \)
   - Extract \( N_{\pi_i} \) number of A- and R-phases with higher memory demand from the jobs of core \( \pi_i \) released in \( W_{li} \).
   - **Sub-case 1:** If the total number of jobs associated to extracted memory phases is greater than \( N_{\pi_i} \), then \( B_{\text{bus}}(W_{li}) \) is given by the sum of all the extracted memory phases.
   - **Sub-case 2:** If the total number of jobs associated to extracted memory phases is equal to \( N_{\pi_i} \), then one A- or R-phase cannot participate in the bus blocking (similarly to Case 2).
   - For sub-case 2, \( B_{\text{bus}}(W_{li}) \) is given by the sum of all the extracted memory phases and then remove the smallest A- or R-phase from the extracted memory phases and add the largest A- or R-phase from the remaining memory phases of core \( \pi_r \) released in \( W_{li} \).

5. Bus-aware WCRT Analysis

- Latest start time of R-phase of \( k^{th} \) job of task \( \tau_i \), of core \( \pi_i \):
  \[
  s_{R_{ki}}^{\text{R}} = C_{pi}^{\text{Max,li}} + \sum_{j \in \text{hep}_{pi}} \left( \eta_j(\pi_i)(W_{li}) \right) C_{pi} + B_{\text{bus}}(W_{li}) + \left( K - 1 \right) C_i + \left( C_i^A + C_i^R \right)
  \]

- WCET of \( \tau_i \):
  \[
  \text{WCET of } \tau_i = \text{Previous jobs of } \tau_i + \text{Bus Blocking until start time of R-phase of } \tau_i
  \]

- Response time of \( k^{th} \) job of task \( \tau_i \), of core \( \pi_i \):
  \[
  R_{ki} = s_{R_{ki}}^{\text{R}} + C_i
  \]

- WCRT of task \( \tau_i \), of core \( \pi_i \):
  \[
  R_{\text{max}} = \max_{k \in [1, \eta_i(\pi_i)(W_{li})]} \left\{ R_{ki} \right\}
  \]

6. Future Work

- Experimental evaluation and comparison with the state of the art.

References