# Towards the Certification of Multicore Platforms in the Avionics Domain

M. Ali Awan*, P. Meumeu Yomsi*, K. Bletsas*, V. Nelis*, E. Tovar*, and P. Souto†

* CISTER - Research Center in Real-Time & Embedded Computing Systems

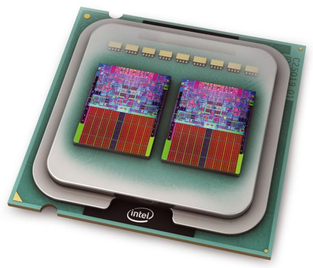
{muaan,pamyo,ksbs,nelis,emt}@isep.ipp.pt

† Universidade do Porto FEUP Faculdade de Engenharia

pfs@fe.up.pt

## Motivation and challenges

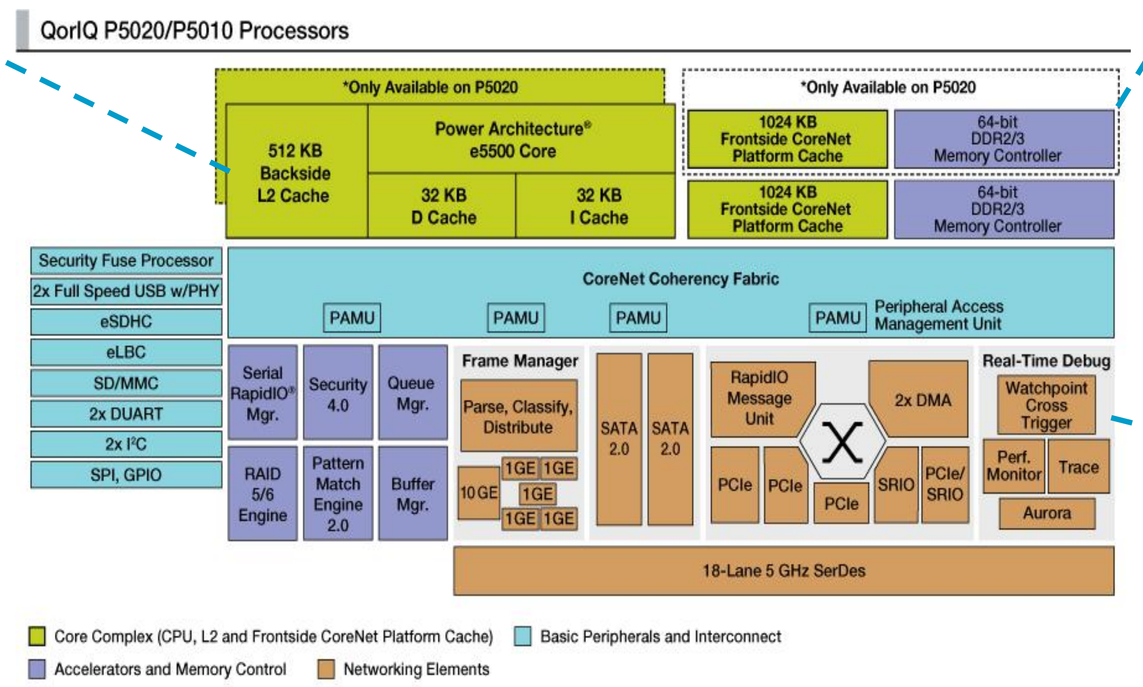
- Demand for extra functionality
- Performance per watt ratio increase
- Multicore paradigm shift
- Resource sharing
- Non-deterministic behavior
- Safety critical applications
- CAST-32 position paper
- Software-based solutions



## Sources of non-determinism

### Caches

- Shared caches
- Effect on WCET
- Preemptions overhead
- Partitioned caches
- Local overhead accounting
- Cache usage profile




### Memory

- Shared memory
- Race conditions
- Data starvation
- Deadlocks
- Live-locks

### I/O Subsystem

- Interact with environment
- Shared I/O devices
- Direct Memory Access (DMA)
- Traffic between cores and memory
- Cache coherency
- DMA interference

## Conclusions

- There is a strong industrial drive towards developing hardware-based solutions
- We firmly believe on the merits of software-based mechanisms
- Partitioned caches is the way forward for safety critical applications
- Cache related preemption delay should be handled locally on each core
- Better bounds can be achieved by differentiating between buffered and non-buffered traffic
- Using scratchpad for allocating I/O data can reduce the interference and coherency issues

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## References

- "Certification authorities software team (cast), position paper (cast- 32) multicore processors," Certification authorities in North and South America, Europe, and Asia, May 2014.

CISTER Research Centre/INESC-TEC
ISEP, Polytechnic Institute of Porto
Rua Dr. Antº Bernardino de Almeida, 431
4200-072 PORTO Portugal
tel: +351-228340502
fax: +351-228340509
http://www.cister.isep.ipp.pt
cister-info@isep.ipp.pt